IN THE CLAIMS.

Following are the claims as currently pending for consideration:

1. (Previously Presented) A computer software product for formal verification of circuits or other finite-state systems, the computer software product having one or more recordable medium having executable instructions stored thereon which, when executed by a processing device, causes the processing device to:

   generate, from a first property, a first assumption including a first state predicate;

   generate, for a model, a first transition relation that includes the first state predicate; and

   reduce the first transition relation according to the first assumption.

2. (Original) The computer software product recited in Claim 1 wherein reducing the first transition relation reduces the size of the model.
3. (Original) The computer software product recited in Claim 1 wherein reducing the first transition relation reduces the computational complexity of evaluating the first property.
4. (Original) The computer software product recited in Claim 1 wherein reducing the first transition relation reduces the number of variables in the model.
5. (Original) The computer software product recited in Claim 1 wherein reducing the first transition relation reduces the number of variables in the first transition relation.
6. (Original) The computer software product recited in Claim 1 wherein the first assumption is generated from an implication structure of the first property.

7. (Original) The computer software product recited in Claim 6 which, when executed by a processing device, further causes the processing device to:

propagate the first assumption to generate a second assumption according to a second property.

8. (Original) The computer software product recited in Claim 7 wherein the second property is a sub-property of the first property.

9. (Original) The computer software product recited in Claim 7 wherein the second property is to be evaluated under the first assumption.

10. (Original) The computer software product recited in Claim 7 wherein the first assumption is propagated only one transition stage to generate the second assumption.

11. (Previously Presented) A verification system for verification of circuits or other finite-state systems, the verification system comprising:

means for producing, from a first property, a first assumption including a first state predicate; and

means for producing a reduced next state function from a first next state function involving the first state predicate by applying the first assumption.

12. (Original) The verification system of Claim 11 wherein the first assumption is produced from the structure of the first property.

13. (Original) The verification system of Claim 12 further comprising:

means for propagating the first assumption according to a second property to generate a second assumption; and

means for producing, for a model, a transition relation that includes the reduced next state function.

14. (Original) The verification system of Claim 13 wherein the second property is a sub-property of the first property.

15. (Original) The verification system of Claim 14 wherein the first assumption is propagated only one transition stage to generate the second assumption.

16. (Previously Presented) A verification system for verification of circuits or other finite-state systems, the verification system comprising:

a recordable medium to store executable instructions;

a processing device to execute executable instruction; and

a plurality of executable instructions to cause the processing device to:

produce, from a first property, a first assumption including a first state predicate;

produce, for a model, a first transition relation that includes the first state predicate; and

reduce the first transition relation according to the first assumption.

17. (Original) The verification system of Claim 16 wherein the first assumption is produced from the logical structure of the first property.

18. (Original) The verification system recited in Claim 17, the plurality of executable instructions further comprising instructions to cause the processing device to:

propagate the first assumption to generate a second assumption according to a second state predicate.

19. (Previously Presented) The verification system recited in Claim 18 wherein the second property is a sub-property of the first property.